Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **D0**
2. **D1**
3. **D2-3**
4. **VCC**
5. **D2**
6. **D3**
7. **NC**
8. **Q3**
9. **Q2**
10. **NC**
11. **GND**
12. **E0-1**
13. **Q1**
14. **Q0**

**.055”**

**.049”**

**2 1 14 13 12**

**3**

**4**

**5 6 7 8 9 10**

**11**

**MASK**

**REF**

**LS 75**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: LS 75**

**APPROVED BY: DK DIE SIZE .049” X .055” DATE: 3/31/16**

**MFG: ON SEMI THICKNESS .013” P/N: 54LS75**

**DG 10.1.2**

#### Rev B, 7/1